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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/042,074

01/08/2002

Dun-Nian Yaung

TS01-450

3909

28112

7590

01/27/2004

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EXAMINER

TRAN, TAN N

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 01/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/042,074

Applicant(s)

YAUNG ET AL.

Examiner

TAN N TRAN

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 January 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a logic circuit region on the chip periphery, and a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements as recited in claims 1,7,13,20,27,34, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-40 are rejected under 35 U.S.C. 103(a) as being unpatentable Applicant' prior Art (APA) in view of Jo (6,379,992)

With regard to claims 1,2,7,8,13,15,20,22,27,29,34,36, APA discloses a semiconductor image sensor chip having a pixel region 20 covering most of the chip and metal region 24 serves as a logic circuit region on the chip peripheral area 22, the pixel region 20 containing an array of

image pixels where for each image pixel, the majority of its area is occupied by a light sensing element 48 and wherein the logic circuit region having the other image pixel circuit elements are arranged in the image pixel periphery 22 without overlapping the image sensing element 48; a number of metal levels (26,28) of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements; a number of second metal levels having each of the functional patterns (26,28) exist only for the chip peripheral logic circuit; a first dielectric layer 44 under the first metal layer 26, an interlevel dielectric layer 40(42) between the functional patterns (26,28) and a passivation layer 34 formed over the last metal level 28. (Note figs. 3,4 of APA).

APA does not disclose the dummy metal patterns cover the pixel region except for the light sensing regions.

However, Jo discloses the optical shielding metal layer 40 serves as the dummy metal patterns cover the pixel region except for the light sensing regions 33. (Note fig. 2G of Jo).

Therefore, it would have been obvious to one of ordinary skill in the art to form the APA's device having the dummy metal patterns cover the pixel region except for the light sensing regions such as taught by Jo in order to prevent light being transmitted into the circuits neighboring the unit pixel.

With regard to claims 3,4,9,10,16,17,23,24,30,31,37,38, Jo discloses the number of metal levels of the first and second types are three. (Note fig. 2G of Jo).

With regard to claims 5,11,18,25,32,39, APA and Jo disclose all the claimed subject matter except for the number of metal levels of the first and second types are composed of either copper, gold, aluminum, cobalt or tungsten or of composite of these metals or of metal

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silicides. However, it would have been obvious to one of ordinary skill in the art to form the number of metal levels of the first and second types are composed of either copper, gold, aluminum, cobalt or tungsten or of composite of these metals or of metal silicides in order to improve the sensitivity of photodiode.

With regard to claims 6,12,19,26,33,40, APA and Jo disclose all the claimed subject matter except for the dielectric and passivation levels are composed of dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride. However, it would have been obvious to one of ordinary skill in the art to form the dielectric and passivation levels are composed of dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride in order to improve the sensitivity of photodiode.

With regard to claims 14,21, Jo discloses the light sensing element 33 is a photodiode. (Note fig. 2G of Jo).

With regard to claims 28,35, APA and Jo disclose all claimed invention as in claim 27, except the light sensing element is an emitter-base junction of a bipolar transistor. However, although APA and Jo do not teach exact the type of the light sensing element as that claimed by Applicant, the type differences are considered obvious design choices and are not patentable unless unobvious or expected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note in re Leshin, 125 USPQ 416.

Conclusion


3. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

Jan 2004


Minhloan Tran
Primary Examiner
Art Unit 2826